

71. (Previously Presented) The method of claim 67, wherein the plurality of control bias voltage signals are substantially proportional to a semiconductor bandgap voltage.

72. (Previously Presented) The method of claim 67, wherein the common mode voltage is substantially proportional to a semiconductor bandgap voltage.

REMARKS

Claims 1-72 are now pending in the application. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

REJECTION UNDER 35 U.S.C. § 112

Claims 21 and 37 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point and distinctly claim the subject matter which Applicant regards as the invention. This rejection is respectfully traversed.

Applicant amended claim 21 to clarify a first bias voltage source to provide the first bias voltage to the first differential amplifier, a second bias voltage source to provide the second bias voltage to the third MOS transistor, and a third bias voltage source to provide the third bias voltage to the second differential amplifier. Applicant amended claim 37 according to the Examiner's suggestion. Applicant respectfully

submits that claims 21 and 37 are now definite. These amendments are not narrowing amendments.

REJECTION UNDER 35 U.S.C. § 102

Claims 18-20 and 41-43 are rejected under 35 U.S.C. § 102(b) as being anticipated by Des Rosiers et al. (U.S. Pat. No. 5,495,184). This rejection is respectfully traversed.

With respect to claim 18, Des Rosiers fails to show, teach, or suggest a second differential amplifier having a second input connected to the third drain and the second source, a third input in communication with a third bias voltage, and an output in communication with the second gate. Des Rosiers does not disclose that the second input is connected to the alleged third drain and second source.

For anticipation to be present under 35 U.S.C. §102(b), there must be no difference between the claimed invention and the reference disclosure as viewed by one skilled in the field of the invention. Scripps Clinic & Res. Found. V. Genentech, Inc., 18 USPQ.2d 1001 (Fed. Cir. 1991). All of the limitations of the claim must be inherent or expressly disclosed and must be arranged as in the claim. Constant v. Advanced Micro-Devices, Inc., 7 USPQ.2d 1057 (Fed. Cir. 1988). Here, Des Rosiers fails to disclose the limitation that the second input of the second differential amplifier is connected to the third drain and the second source.

As shown in an exemplary embodiment in FIG. 4b, a compensation circuit includes a second MOS transistor M8 having a second source and a third MOS transistor M9 having a third drain. A second differential amplifier U1 has a second input connected to the third drain and the second source (i.e. the input Vn connected at a node between M8 and M9).

As best understood by Applicant, Des Rosiers does not disclose this structure. For example, the Examiner alleges that FIG. 4 of Des Rosiers discloses a second differential amplifier OP2, a second MOS transistor N4, and a third MOS transistor N3. Applicant respectfully notes that the alleged second input of the second differential amplifier OP2 is connected to a node V_{OL2} . **The node V_{OL2} (and therefore the second input) is connected to a second drain of the second MOS transistor N4. The second input is not connected to the source S of the second MOS transistor N4 (i.e. the alleged second source), and is similarly not connected to the drain D of the third MOS transistor N3 (i.e. the alleged third drain).**

Applicant respectfully submits that Des Rosiers fails to show, teach, or suggest a second differential amplifier having a second input connected to the third drain and the second source. Claim 18, as well as its dependent claims, should be allowable for at least the above reasons.

With respect to claim 41, Des Rosiers fails to show, teach, or suggest a second differential amplifier means for amplifying as a first input the third drain and the second source.

The Examiner alleges that claim 41 recites similar limitations as claim 18. Applicant respectfully notes that claim 41 recites second differential amplifier means for **amplifying as a first input the third drain and the second source**. In other words, the second differential amplifier means U1 amplifies the third drain and the second source as described above with respect to claim 18 (as shown in FIG. 4b. Des Rosiers does not disclose this structure. In contrast, Des Rosiers appears to disclose amplifying, as a first input, a second drain of the second MOS transistor N4. The alleged second differential amplifying means OP2 is not connected to either of the second source or the third drain and, as such, does not disclose **amplifying as a first input the third drain and the second source**.

Applicant respectfully submits that claim 41, as well as its dependent claims, should be allowable for at least the above reasons.

Claims 22, 23, 25, 29, 32, and 34 are rejected under 35 U.S.C. § 102(b) as being anticipated by Nagaraj et al. (U.S. Pat. No. 5,642,077). This rejection is respectfully traversed.

With respect to claim 22, Nagaraj fails to show, teach, or suggest analog integrated function means for providing first and second output signals responsive to a first differential input signal and a second differential input. In particular, Nagaraj fails to disclose the limitation of first and second output signals responsive to **a first differential input signal and a second differential input signal**.

As shown in an exemplary embodiment in FIG. 4a, an analog function circuit includes a first differential input signal (i.e. the pair of inputs V_x) and a second differential input signal (i.e. the pair of inputs V_y). Applicant respectfully notes that **a**

differential input signal is a difference between at least a pair of input signals as shown in FIG. 4a.

Nagaraj does not appear to disclose this limitation. The Examiner relies on FIG. 1 of Nagaraj to disclose analog integrated function means (elements 122, 120, 140, and 104). Applicant respectfully notes that the alleged analog integrated function means does not provide first and second output signals responsive to **a first differential input signal and a second differential input signal** as claim 22 recites. In other words, Applicant's claim 22 recites two differential input signals (i.e. two differences between respective pairs of inputs V_x and V_y as shown in FIG. 4a) and Nagaraj discloses, at best, only a pair of inputs.

Further, Applicant's claim 22 recites compensation means for generating the compensation control signal to compensate for changes due to temperature and manufacturing variations. The Examiner alleges that Nagaraj discloses a compensation circuit at 142 and 150. Applicant respectfully notes that Nagaraj appears to be absent of any teaching or suggestion that these elements generate a compensation control **signal to compensate for changes due to temperature and manufacturing variations**. Nagaraj appears to be completely silent with respect to compensating for temperature and manufacturing variations.

Applicant respectfully submits that claim 22, as well as its dependent claims, should be allowable for at least the above reasons. Claim 32, as well as its dependent claims, should be allowable for at least similar reasons.

❖ ❖ ❖

REJECTION UNDER 35 U.S.C. § 103

Claims 31 and 45-72 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Nagaraj et al. (U.S. Pat. No. 5,642,077). This rejection is respectfully traversed.

With respect to claim 45, Nagaraj fails to show, teach, or suggest a biasing circuit in communication with a common mode node of the differential loading device and an input of the compensation circuit, wherein the biasing circuit provides a common mode voltage to the common mode node of the differential loading device and the compensation circuit, and wherein the common mode voltage is independent of temperature and manufacturing process variations.

The Examiner acknowledges that Nagaraj fails to disclose a biasing circuit that provides a common mode voltage that is independent of temperature and manufacturing process variations. Instead, the Examiner alleges that it is known that bandgap voltage is temperature independent and therefore it would have been obvious to one having ordinary skill in the art to use bandgap voltage to generate temperature independent voltage. Applicant respectfully submits that Nagaraj appears to be absent of any teaching or suggestion of making the alleged common mode voltage independent of temperature and manufacturing process variations, and that the Examiner provides NO references that teach a common mode voltage that is independent of temperature and manufacturing process variations.

Applicant respectfully asserts that the Examiner has failed to clearly and particularly support his alleged motivation to modify Nagaraj using actual evidence as required. According to established mandates of the patent laws, “[t]o establish a prima

facie case of obviousness . . . there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings.” **M.P.E.P. § 2142.** “There are three possible sources for a motivation to combine references: the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art.” **M.P.E.P. § 2143.01.**

“The motivation, suggestion or teaching may come explicitly from statements in the prior art, the knowledge of one of ordinary skill in the art, or, in some cases the nature of the problem to be solved.” *In re Kotzab*, 217 F.3d 1365, 1370, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000). The showing must be “clear and particular, and it must be supported by **actual evidence**.” *Teleflex, Inc. v. Ficosa North American Corp.*, 299 F.3d 1313, 1334, 63 U.S.P.Q.2d 1374, 1387 (Fed. Cir. 2002) (quoting *In re Dembiczak*, 175 F.3d 994, 999, 50 U.S.P.Q.2d 1614, 1617 (Fed. Cir. 1999)) (emphasis added). It is not sufficient to rely on “common sense and common knowledge,” as there must be specific evidence to support the motivation. *In re Lee*, 277 F.3d. 1338, 1344-45, 61 U.S.P.Q.2d 1430, 1434-35 (Fed. Cir. 2002)]. It is respectfully submitted that the Patent Office has not made a legally sufficient showing of a motivation to combine based on actual, specific, evidence.

Rather, according to M.P.E.P. § 2142, “[t]o reach a proper determination under 35 U.S.C. 103, . . . impermissible hindsight must be avoided and the legal conclusion [of obviousness] must be reached on the basis of the facts gleaned from the prior art.” Furthermore, according to M.P.E.P. § 2143.01, “[t]he mere fact that references can be . . . modified does not render the resultant combination obvious unless the prior art also

suggests the desirability of [such modification].” **In re Mills**, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990). Since the Patent Office has offered no proper support or motivation for combining the references, it is respectfully submitted that the rejection based on obviousness is clearly and unequivocally founded upon “knowledge gleaned only from applicant’s disclosure.” **M.P.E.P. § 2145**. Consequently, it is respectfully submitted that the rejection entails hindsight and is, therefore, improper.

Applicant respectfully submits that claim 45, as well as its dependent claims, should be allowable for at least the above reasons. Claims 56 and 67, as well as their corresponding dependent claims, should be allowable for at least similar reasons.

ALLOWABLE SUBJECT MATTER


Claims 1-17 are allowed. The Examiner states that claims 26-28, 30, and 35-40 would be allowable if rewritten in independent form. Applicant thanks the Examiner for the allowable subject matter. Accordingly, Applicant elects to defer amending the claims into independent form until after the above remarks are considered.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action and the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

Dated: November 29, 2006

By: 
Michael D. Wiggins
Reg. No. 34,754

HARNESS, DICKEY & PIERCE, P.L.C.
P.O. Box 828
Bloomfield Hills, Michigan 48303
(248) 641-1600

MDW/mp/dma